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10/799,852	03/12/2004	Isamu Miyanishi	2271/71532	2074

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EXAMINER	
ZAMAN, FAISAL M	
ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,852	MIYANISHI ET AL.	
	Examiner	Art Unit	
	Faisal M. Zaman	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19,20 and 22-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,20 and 22-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 22-24 and 30-33** are rejected under 35 U.S.C. 102(e) as being anticipated by Chu et al. ("Chu") (U.S. Patent Application Publication No. 2004/0015731).

Regarding Claims 22 and 31, Chu discloses an optical disk drive apparatus (Figure 2, item 220 with item 2 or alternatively Figure 3, item 300), comprising:

An optical disk drive mechanism (Figure 3, item 301) configured to read data from an optical disk medium (Figure 3, item 360, paragraph 0010);

A register circuit (Figure 2, item 140 or alternatively Figure 3, items 320/332) including a plurality of registers configured to store data read by said optical disk drive mechanism from said optical disk medium to be transferred from the optical disk drive apparatus to a host computer (Figure 3, item 10, paragraph 0036);

A first memory configured to store first information indicating specific addresses of corresponding specified registers in the register circuit and representing an access

executed by the host computer to the optical disk drive mechanism for a data transfer (Figure 3, item 420, paragraph 0033; i.e., upon receiving a read command from host 10, memory 420 stores a Logical Block Address [LBA]);

A second memory configured to store second information, received by said second memory in association with the first information stored in the first memory and corresponding to said data ready by said optical disk drive mechanism from said optical disk medium and to be transferred from the optical disk drive apparatus to said host computer, to be written into the specified registers at the specific addresses indicated by the first information stored in the first memory (Figure 3, item 420, paragraph 0033; i.e., read data from optical disk medium 360 is buffered in memory 420); and

A control circuit configured to perform an information writing operation for writing the first information and the second information into the first memory and the second memory, respectively, in chronological order of accesses executed, in connection with said data read by said optical disk drive mechanism from said optical disk medium and to be transferred from the optical disk drive apparatus to said host computer (Figure 3, item 400, paragraph 0033).

Regarding Claim 23, 24, 32, and 33, Chu discloses wherein the control circuit performs the information writing and reading operation for writing and reading the first information into the first memory and the second information into the second memory in chronological order of accesses executed, when an operation mode of the communications interface apparatus is changed from a low power consumption mode to

a regular operation mode (paragraph 0033; i.e., HDD 300 state is changed from eData mode to Active mode).

Regarding Claim 30, Chu discloses wherein the register circuit, the first and second memories, and the control circuit are integrated into a single integrated chip (Figure 3, item 301).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 25, 26, 29, and 34-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu as applied to Claim 22 above, and further in view of Yamada et al. ("Yamada") (U.S. Patent No. 6,470,439).

Chu discloses the invention substantially as claimed.

Regarding Claims 25 and 35, Chu discloses wherein the control circuit conducts the information writing operations with respect to the first and second memories in synchronism with each other and conducts the information reading operations with respect to the first and second memories in synchronism with each other (Chu, paragraph 0033).

In same field of endeavor (e.g. the use of a memory control circuit in controlling memory used in various electronic devices), Yamada teaches the following limitation, which Chu does not expressly disclose:

Wherein a memory comprises a first-in and first-out memory (Yamada, title, abstract) including a specific number of buffer areas into which data from an external device is written (Yamada, Column 3, lines 18-31).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have incorporated Yamada's teachings of the use of a memory control circuit in controlling memory used in various electronic devices with the teachings of Chu, for the purpose of providing a FIFO memory control circuit in which the amount of effective data in a memory can be correctly counted so that when the frequencies of a read clock and a write clock are different, data is prevented from being lost by being overwritten, and data is prevented from being read out twice (see Yamada, Column 6, lines 18-22).

Regarding Claims 26 and 36, Chu discloses wherein the control circuit performs the information writing and reading operation for writing and reading the first information into the first memory and the second information into the second memory in chronological order of accesses executed when an operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode (Chu, paragraph 0033; i.e., HDD 300 state is changed from eData mode to Active mode).

Chu does not expressly disclose wherein the information writing and reading operation is performed without buffering the first and second information in the first-in and first-out memories in an event that the respective first-in and first-out memories of the first and second memories are in a memory empty state after the first and second information stored in the respective first-in and first-out memories of the first and second memories, respectively, are transferred to the register circuit when the operation mode of the communications interface apparatus is changed from a low power consumption mode to a regular operation mode.

In the same field of endeavor, Yamada teaches wherein data is not written (ie. is not buffered) into a FIFO memory in the event that a FULL signal is sent from the memory control circuit, indicating the FIFO memory is full (Yamada, Column 4, lines 12-22).

The motivation that was utilized in the combination of Claim 25, super, applies equally as well to Claims 26 and 36.

Regarding Claims 29 and 34, Yamada discloses the following, which Chu does not expressly disclose:

Wherein the control circuit accesses the first and second memories in synchronism with a first clock signal for the information writing operation and a second clock signal for the information reading operation (Yamada, Column 3, lines 26-31), and wherein a first frequency of the first clock signal is greater than a second frequency of the second clock signal (Yamada, Column 4, lines 43-52).

The motivation that was utilized in the combination of Claim 25, super, applies equally as well to Claims 29 and 34.

5. **Claims 27-28 and 37-38** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu and Yamada as applied to Claim 25 above (hereinafter "Chu-Yamada"), and further in view of Chuang et al. ("Chuang") (U.S. Patent No. 6,502,159).

Chu-Yamada discloses the communications interface apparatus according to Claim 26, as described above.

Regarding Claims 27 and 37, Chu-Yamada does not expressly disclose wherein each of the first and second memories comprises a selection circuit configured to select one of (i) a first data path for the first and second information not via the first and second memories and (ii) a second data path for the first and second information via the respective first and second memories, on an exclusive basis according to a control signal from the control circuit and to output corresponding data to the register circuit through the selected one of the first and second data paths.

In the same field of endeavor (e.g. data transfers between a disk drive apparatus and a host computer), Chuang teaches wherein a circuit (Chuang, Figure 2, item 105, Column 4, lines 22-23) comprises a selection circuit (Chuang, Figure 3, item 120, Column 4, lines 36-50) configured to select one of (i) a first data path for information not via a memory (Chuang, Table 2, Column 4, lines 26-29) and (ii) a second data path for the information via a memory (Chuang, Table 1, Column 4, lines 23-25), on an exclusive basis according to a control signal from a control circuit (Chuang, Figure 2, item 12,

Column 3, lines 56-60) and to output corresponding data to a circuit (Chuang, Figure 3, item 57, Column 3, lines 56-60) through the selected one of the first and second data paths.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Chuang's teachings of data transfers between a disk drive apparatus and a host computer with the teachings of Chu-Yamada, for the purpose of greatly reducing system memory usage and bus utilization (see Chuang, Column 3, lines 52-55) and to reduce unnecessary data flow in the system and unnecessary consumption of system resources (see Chuang, Column 3, lines 60-64).

Regarding Claims 28 and 38, Chu-Yamada discloses wherein the control circuit comprises:

A data writing circuit block configured to write the first and second information into the first and second memories, respectively, in accordance with an access performed by the host computer (Chu, Figure 3, item 400);

A data reading circuit block configured to start reading the first and second information from the first and second memories, respectively, upon a time the write control circuit block starts writing the first and second information into the first and second memories, respectively (Chu, Figure 3, item 400);

A status detecting circuit block configured to detect memory statuses of the first-in and first-out memories included in the respective first and second memories and to

output a status signal representing the memory statuses detected (Chu, Figure 3, item 338); and

A selection control circuit block configured to control accesses to the respective first and second memories in accordance with a status as to whether the operation mode of the communications interface apparatus is the low power consumption mode and the status signal output from the status detecting circuit block (Chu, paragraphs 0032-0033; i.e., data from host 1 is only buffered in write cache 130 [Figure 2] or RAM 420 [Figure 3] when the HDD 300 is in eData [i.e., idle] mode).

Chu-Yamada does not expressly disclose wherein the selection control circuit block is configured to control the selection circuits included in the respective first and second memories.

In the same field of endeavor, Chuang teaches wherein a selection control circuit block (Chuang, Figure 2, item 105, Column 4, lines 22-23) is configured to control the selection circuit (Chuang, Figure 3, item 120, Column 4, lines 36-50) included in a circuit in accordance with a status from a control circuit (Chuang, Figure 2, item 12, Column 3, lines 56-60).

The motivation used in the combination of Claim 27, super, applies equally as well to Claims 28 and 38.

6. **Claims 19, 20, 39, and 40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chu and Mirov et al. ("Mirov") (U.S. Patent No. 6,528,974).

Regarding Claim 19, Chu teaches an optical disk drive apparatus (Chu, Figure 1, item 220 with item 2, or alternatively Figure 3, item 300, paragraph 0010), comprising:

An optical disk drive mechanism (Chu, Figure 3, item 301);

An interface circuit (Chu, Figure 2, item 220) for interfacing communications, between the optical disk drive mechanism and a host computer (Chu, Figure 3, item 10), the interfacing circuit comprising:

An input terminal for receiving data sent from the host computer (Chu, Figure 2, item 110);

A data processor configured to perform a predetermined data processing operation to the data received through the input terminal (Chu, Figure 3, item 314); and

A clock generator configured to generate a clock signal with which the data processor performs the predetermined data processing operation (Chu, Figure 3, item 318);

A buffering circuit block configured to buffer the data received through the input terminal of the disk drive apparatus from the host computer (Chu, Figure 2, item 130), the buffering circuit block including:

A first data transfer path configured to transfer the data received through the input terminal to the data processor not via a memory, and a second data transfer path configured to transfer the data received through the input terminal to the data processor via a memory (Chu, paragraphs 0032-0033; i.e., data from host 1 is only buffered in

write cache 130 [Figure 2] or RAM 420 [Figure 3] when the HDD 300 is in eData [i.e., idle] mode); and

A path selection controller configured to control the buffering circuit block to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode (Chu, Figure 2, item 120 or alternatively Figure 3, item 400).

Chu does not expressly teach an operation mode changer configured to control the clock generator to reduce a frequency of the clock signal to a non-zero value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode.

In the same field of endeavor (e.g. reading data from a disc for use by a computer), Mirov teaches an operation mode changer configured to control a clock generator to reduce a frequency of a clock signal to a non-zero value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode (Mirov, Column 4, lines 24-41).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have combined Mirov's teachings of reading data from a disc for use by a computer to the teachings of Chu, for the purpose of providing a disc apparatus having a reduced power consumption during a sleep mode for greater efficiency in a computing system.

Regarding Claim 20, Chu teaches wherein the path selection controller selects one of the first and second data transfer paths for a write operation (Chu, paragraphs 0032-0033).

Regarding Claim 39, Mirov teaches wherein in a regular operation mode, a first clock signal of a first frequency of said predetermined value is supplied from the clock generator to a data processor (Mirov, Figure 1, item 104), and in said low power consumption mode, a second clock signal of a second frequency of said non-zero value is supplied from the clock generator to the data processor (Mirov, Column 4, lines 24-41).

The motivation that was used in the combination of Claim 19, super, applies equally as well to Claim 39.

Regarding Claim 40, Mirov teaches wherein the clock generator includes a clock generation circuit configured to generate concurrently a plurality of clock signals of respective non-zero frequencies, and one of said plurality of clock signals of respective non-zero frequencies is selected to be output as said clock signal of said clock generator (Mirov, Column 5, lines 21-45).

The motivation that was used in the combination of Claim 19, super, applies equally as well to Claim 40.

Response to Arguments

7. Applicant's arguments filed 7/17/2008 have been fully considered but they are not persuasive.

With regards to Claim 22, Applicant argues that "the 16-bit register 320 of Chu … is not a register circuit including a plurality of registers." However, the examiner has interpreted the "register circuit" to include both register 320 and register 332, since it can be seen that both of these registers receive information from HDC 312.

Also with regards to Claim 22, Applicant argues that the "LBA [logical block address] counter has nothing to do with specific addresses of the 16-bit data register 320 of Chu", and "the LBA counter of Chu is used to store the starting address of the data in the memory 420." The examiner disagrees. Contrary to Applicant's argument, the LBA counter of Chu does in fact store the addresses of the corresponding registers in the register circuit (i.e., the addresses in which the read data will be stored after it is buffered). The LBA counter is "used to store the starting address of the data" (paragraph 0038). Since the data which is intended to be sent to the host 10 is stored in the data register 320, the logical block addresses that are stored in memory 420 do in fact point to the "specific addresses of corresponding specified registers (i.e., register 320) in the register circuit".

Finally with regards to Claim 22, Applicant argues that "the state machine 400 of Chu … does not perform an information writing operation for writing the first information and the second information into the first and second memory, respectively, in chronological order of access executed." The examiner disagrees. Contrary to

Applicant's argument, the state machine 400 does in fact store the first information (i.e., the logical block address of register 320) in the first memory (i.e., memory 420) and the second information (i.e., data that is being read from the optical disk 360) into a second memory (i.e., the read data buffer within memory 420). Furthermore, it is stated in Chu that if a cache hit does not occur upon receiving a read request, the state machine 400 awakes the HDD 300 and writes the appropriate read data into the memory 420, see paragraph 0036. Therefore, it is clear that state machine 400 writes data into the appropriate locations in chronological order of access executed since it retrieves data from the disk in the order in which the read commands were received from the host 10.

With regards to Claim 19, Applicant argues that "Chu … does not disclose or suggest a path selection controller configured to control the buffering circuit block to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode…". The examiner disagrees. Contrary to Applicant's argument, the state machine 400 (equated to the claimed "path selection controller") in Chu does in fact select between utilizing a write data buffer (i.e., the "second data transfer path") and not utilizing the write data buffer (i.e., the "first data transfer path"). In paragraph 0033, lines 1-5, Chu discloses that the state machine 400 only configures memory 420 to include a write data buffer when the system is eData mode (i.e., a low power consumption mode). Accordingly, since the write data buffer within memory 420 is equated to the claimed "memory", it is clear that the state machine 400 selects between using the "memory" and not using the "memory" (i.e., can select between the two claimed data transfer paths) based on the

type of power consumption mode the system is currently operating in (i.e., normal or eData mode).

Therefore, the claims stand as previously rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal M. Zaman whose telephone number is (571)272-6495. The examiner can normally be reached on Monday thru Friday, 8 am - 5:30 pm, alternate Fridays, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/F. M. Z./
Examiner, Art Unit 2111

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